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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,585	11/24/2003	Erik R. Altman	YOR920030405US1	5059

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EXAMINER	
LAI, VINCENT	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,585	ALTMAN ET AL.	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Hazm. Fleming

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
8/7/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on March 29, 2004 was considered by the examiner.

Response to Amendment

2. Acknowledgment is made for the amendment to the specification and claims.

3. Previous objections to the drawings and claims are withdrawn after considering amendments.

Claim Objections

4. Claim 2 is objected to because of the following informalities: An extraneous "to" is present in the amendment portion of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application

> by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-4, 6-16, 18, 22-25, 27-36, 39, and 43-44 are rejected under 35 U.S.C. 102(e) as being anticipated by Christie (U.S. Patent # 6,877,084 B1).

As per claim 1, Christie discloses a digital data processor (See column 4, lines 59-63) comprising an instruction unit (See column 5, lines 34-44), said instruction unit comprising a code page (See column 7, lines 36-45: Ability to page indicates a code page) that is partitioned for storing in a first section thereof a plurality of instruction words (See figure 7: Standard Register Set 84) and, in association with at least one instruction word, in a second section thereof an extension to said at least one instruction word (See figure 7: Extended Register Set).

As per claim 2, Christie discloses where said first section is comprised of a first plurality of contiguous storage locations, and where said second section is comprised of a second plurality of contiguous storage locations (See figure 7: Registers are

contiguous storage locations), and where at least one instruction word and said extension to said at least one instruction word are one of fixed length and variable length program instructions (See column 3, lines 11-19).

As per claim 3, Christie discloses further comprising at least one page table entry bit having a state for indicating, on a code page by code page basis, whether the code page is partitioned into said first and second sections for storing instruction words and at, least one instruction word extension, or whether the code page is comprised instead of a single section storing only instruction words (See figure 5 and column 5, line 66- column 6, line 10: A signal is sent to indicate what mode is being used).

As per claim 4, Christie discloses where said at least one page table entry bit is output from a translation lookaside buffer (TLB) (See column 7, lines 44-45).

As per claim 6, Christie discloses further comprising address circuitry for addressing an instruction word in said first section using a current instruction address, while simultaneously addressing an extension to said instruction word at a fixed offset from said current instruction address. (See column 5, line 66- column 6, line 10: In the extension mode, all bits are accessed at once).

As per claim 7, Christie discloses where at least some of the second storage locations are not allocated for storing instruction word extensions (See figure 7: The extended register set is not limited to just instructions).

As per claim 8, Christie discloses where said at least some of the second storage locations that are not allocated for storing instruction word extensions are allocated instead for storing at least one of constant values, security information, and error detection and/or correction information for the code page (See figure 7: The extended register set is not limited to just instructions and can store anything registers are meant to store).

As per claim 9, Christie discloses further comprising an address comparator for detecting when program execution has reached the end of the first section for ensuring that a next instruction address is not contained in the second section (See column 7, lines 36-45: This is done with paging).

As per claim 10, Christie teaches where each instruction word has a width of x bits (See column 3, lines 11-19: Instruction length is variable, but explicitly discloses as 32-bits), where each extension has a width of y bits (See column 3, lines 11-19: Instruction length is variable, but discloses as up to 32-bits) where x=n(8-bits) (See column 3, lines 11-19: 32-bits would mean n = 4), where y=m(8-bits), where n is an

integer greater than one, and where m has a value less than one, equal to one, or greater than one (See column 3, lines 11-19: Extension is variable).

As per claim 11, Christie discloses further comprising circuitry, coupled to an output of said code page, to combine an addressed instruction word read out of said code page with a corresponding instruction word extension that is also read out of said code page (See column 5, line 66- column 6, line 10: In the extension mode, all bits are accessed at once).

As per claim 12, Christie discloses where said combining circuitry comprises an instruction cache having a bit width w at least equal to a width of an instruction word plus a width of the instruction word extension (See column 5, line 66- column 6, line 10: The registers will be able to store the instructions).

As per claim 13, Christie discloses where said combining circuitry comprises an instruction cache having a bit width w at least equal to a width of an instruction word plus a width of the instruction word extension (See column 5, line 66- column 6, line 10: The registers will be able to store the instructions), said instruction cache having an output coupled to an input stage of an instruction pipeline (See figure 7), said input stage having a bit width of w (See column 3, lines 11-19: Instruction length is variable).

As per claim 14, Christie discloses where said combining circuitry comprises an input stage of an instruction pipeline (See figure 7).

As per claim 15, Christie discloses where said combining circuitry comprises an instruction decode stage of an instruction pipeline (See figure 7).

As per claim 16, Christie discloses further comprising circuitry, coupled to an output of said code page, to selectively combine, in response to the state of said at least one page table entry bit, an addressed instruction word read out of said code page with a corresponding instruction word extension that is also read out of said code page (See column 5, line 66- column 6, line 10: In the extension mode, all bits are accessed at once).

As per claim 18, Christie discloses where said combining circuitry comprises an instruction decode stage of an instruction pipeline (See figure 7).

As per claim 22, Christie discloses a method to operate an instruction unit (See column 5, lines 34-44) having a code page (See column 7, lines 36-45: Ability to page indicates a code page), comprising:

partitioning said code page (See column 73, lines 28-30: Discloses the existence of code pages) into at least two sections (See figure 7: Standard Register Set 84 and Extended Register Set 86);

and storing in a first section thereof a plurality of instruction words and, in association with at least one instruction word, in a second section thereof an extension to said at least one instruction word (See figure 7).

As per claim 23, Christie discloses where said first section is comprised of a first plurality of contiguous storage locations, and where said second section is comprised of a second plurality of contiguous storage locations (See figure 7: Registers are contiguous storage locations), and where said program instructions are one of fixed length and variable length program instructions (See column 3, lines 11-19).

As per claim 24, Christie discloses further comprising setting a state of at least one page table entry bit for indicating, on a code page by code page basis, whether the code page is partitioned into said first and second sections for storing instruction words and at, least one instruction word extension, or whether the code page is comprised instead of a single section storing only instruction words (See figure 5 and column 5, line 66- column 6, line 10: A signal is sent to indicate what mode is being used).

As per claim 25, Christie discloses further comprising outputting said at least one page table entry bit from translation lookaside buffer (TLB) (See column 7, lines 44-45).

As per claim 27, Christie discloses further comprising addressing an instruction word in said first section using a current instruction address, while simultaneously

addressing an extension to said instruction word at a fixed offset from said current instruction address. (See column 5, line 66- column 6, line 10: In the extension mode, all bits are accessed at once)

As per claim 28, Christie discloses where at least some of the second storage locations are not allocated for storing instruction word extensions (See figure 7: The extended register set is not limited to just instructions).

As per claim 29, Christie discloses where said at least some of the second storage locations that are not allocated for storing instruction word extensions are allocated instead for storing at least one of constant values, security information, and error detection and/or correction information for the code page (See figure 7: The extended register set is not limited to just instructions and can store anything registers are meant to store).

As per claim 30, Christie discloses further comprising detecting when program execution has reached the end of the first section for ensuring that a next instruction address is not contained in the second section (See column 7, lines 36-45: This is done with paging).

As per claim 31, Christie teaches where each instruction word has a width of x bits (See column 3, lines 11-19: Instruction length is variable, but explicitly discloses as

32-bits), where each extension has a width of y bits (See column 3, lines 11-19: Instruction length is variable, but discloses as up to 32-bits) where x=n(8-bits) (See column 3, lines 11-19: 32-bits would mean n = 4), where y=m(8-bits), where n is an integer greater than one, and where m has a value less than one, equal to one, or greater than one (See column 3, lines 11-19: Extension is variable).

As per claim 32, Christie discloses further comprising circuitry combining an addressed instruction word read out of said code page with a corresponding instruction word extension that is also read out of said code page (See column 5, line 66- column 6, line 10: In the extension mode, all bits are accessed at once).

As per claim 33, Christie discloses where combining operates an instruction cache having a bit width w at least equal to a width of an instruction word plus a width of the instruction word extension (See column 5, line 66- column 6, line 10: The registers will be able to store the instructions).

As per claim 34, Christie discloses where combining operates an instruction cache having a bit width w at least equal to a width of an instruction word plus a width of the instruction word extension (See column 5, line 66- column 6, line 10: The registers will be able to store the instructions), said instruction cache having an output coupled to an input stage of an instruction pipeline (See figure 7), said input stage having a bit width of w (See column 3, lines 11-19: Instruction length is variable).

As per claim 35, Christie discloses where combining occurs at an input stage of an instruction pipeline (See figure 7).

As per claim 36, Christie discloses where combining occurs at an instruction decode stage of an instruction pipeline (See figure 7).

As per claim 37, Christie discloses further comprising circuitry, in response to the state of said at least one page table entry bit, an addressed instruction word read out of said code page with a corresponding instruction word extension that is also read out of said code page (See column 5, line 66- column 6, line 10: In the extension mode, all bits are accessed at once).

As per claim 39, Christie discloses where selectively combining circuitry comprises operating an instruction decode stage of an instruction pipeline (See figure 7).

As per claim 43, Christie discloses a computer program stored on a computer readable medium, said computer program comprising instructions for use with an instruction unit having a code page (See column 7, lines 36-45: Ability to page indicates a code page), comprising:

computer program code (See column 5, lines 58-65) for partitioning said code page into at least two sections (See figure 7) for storing in a first section thereof a plurality of instruction words and, in association with at least one instruction word, for storing in a second section thereof an extension to said at least one instruction word (See figure 7);

and computer program code for setting a state of at least one page table entry bit for indicating, on a code page by code page basis, whether the code page is partitioned into said first and second sections for storing instruction words and at least one instruction word extension, or whether the code page is comprised instead of a single section storing only instruction words (See figure 5 and column 5, line 66- column 6, line 10: A signal is sent to indicate what mode is being used).

As per claim 44, Yates, Jr. et al discloses further comprising computer program code for ensuring that a last instruction in said first section is a branch instruction the execution of which does not specify a target address that lies in the second section (See column 63, lines 18-21: It is recognized that page straddling branches will result in errors and thus have safeguards against the errors).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5, 17, 19-21, 26, 38, and 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Christie (U.S. Patent # 6,877,084 B1) in view of Yates, Jr. et al (U.S. Patent # 6,397,379 B1), herein referred to as Yates.

As per claim 5, Christie discloses the digital data processor as in claim 3.

Christie does not disclose an address fault circuitry.

Yates does discloses further comprising address fault circuitry for determining, in accordance with a state of the at least one page table entry bit, whether a generated instruction address is a valid address for the code page (See column 74, lines 35-47: Probing is done to determine validity of addresses).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Christie with Yates because an address fault circuitry is necessary when an address is composed from two separate entities and it is very likely that Christie already employs similar functionality in the memory management unit (See Christie column 7, lines 36-40), Christie does not explicitly disclose such a function. Yates does and one having ordinary skill in the art at the time the invention was made would appreciate such a function and would apply it to Christie.

As per claim 17, Christie discloses the digital data processor as in claim 16.

Christie does not disclose multiplexers.

Yates does discloses where said combining circuitry comprises a multiplexer (Mux 784, see figure 7H) having a first set of inputs coupled to an instruction word extension output of said code page and a second set of inputs coupled to an invalid instruction word extension (See figure 7H: The mux 784 takes in multiple sectors and chooses which sector 722 to output).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Christie with Yates to incorporate multiplexers because multiplexers are recognized as one popular manner into which to select something from a set of values. It is very possible that Christie does intend to include multiplexers as it is a common device used by one having ordinary skill in the art at the time the invention was made but does not disclose the use of them. Yates does and one having ordinary skill in the art at the time the invention was made would appreciate such a device and would apply it to Christie.

As per claim 19, Christie does disclose the digital data processor as in claim 1.

Christie does not disclose using RISC instructions.

Yates does disclose where said instructions comprise Reduced Instruction Set Computer (RISC) instruction words (See column 22, 21-25: The processor disclosed is a RISC processor and thus will handle RISC instructions).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Christie with Yates a RISC instruction set was desired. Christie discloses a CISC instruction set as evidenced by the disclosure of an

x86 instruction set (See Christie column 3, lines 31-33) and although it is very likely that the CISC instruction set is able to handle the RISC instruction set, Yates does explicitly disclose a RISC instruction set.

As per claim 20, Christie does disclose the digital data processor as in claim 19.

Christie does not disclose using RISC instructions.

Yates does disclose where said instruction words (See column 22, 21-25: The processor disclosed is a RISC processor and thus will handle RISC instructions) have a width of 32-bits (See column 38, lines 61-65: Yates, Jr. et al discloses a 64-bit processor. It is inherent that such processors are backwards compatible and can handle standard bit size instructions as well as variable length instructions), where said extension to said at least one instruction word has a width of 8-bits (See column 24, lines 3-7: Variable length instructions are can be viewed as regular length instructions with extensions, include ones of 8-bits).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Christie with Yates a RISC instruction set was desired. Christie discloses a CISC instruction set as evidenced by the disclosure of an x86 instruction set (See Christie column 3, lines 31-33) and although it is very likely that the CISC instruction set is able to handle the RISC instruction set, Yates does explicitly disclose a RISC instruction set.

As per claim 21, Christie does disclose the digital data processor as in claim 20.

Christie does not disclose using RISC instructions.

Yates does disclose where said code page has a storage capacity of 4096 bytes (See column 61, lines 49-50), where said first section comprises 3072 bytes, and where said second section comprises 1024 bytes (See column 2, lines 36-49: Sections in pages are determined by flags and thus can be set to partition the 4096 bytes into 3072 and 1024 bytes).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Christie with Yates a RISC instruction set was desired. Christie discloses a CISC instruction set as evidenced by the disclosure of an x86 instruction set (See Christie column 3, lines 31-33) and although it is very likely that the CISC instruction set is able to handle the RISC instruction set, Yates does explicitly disclose a RISC instruction set.

As per claim 26, Christie discloses the digital data processor as in claim 24.

Christie does not disclose an address fault circuitry.

Yates does discloses further comprising determining, in accordance with a state of the at least one page table entry bit, whether a generated instruction address is a valid address for the code page (See column 74, lines 35-47: Probing is done to determine validity of addresses).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Christie with Yates because an address fault circuitry is necessary when an address is composed from two separate entities and it is

very likely that Christie already employs similar functionality in the memory management unit (See Christie column 7, lines 36-40), Christie does not explicitly disclose such a function. Yates does and one having ordinary skill in the art at the time the invention was made would appreciate such a function and would apply it to Christie.

As per claim 38, Christie discloses the digital data processor as in claim 37.

Christie does not disclose multiplexers.

Yates does discloses where selectively combining comprises operating a multiplexer (Mux 784, see figure 7H) having a first set of inputs coupled to an instruction word extension output of said code page and a second set of inputs coupled to an invalid instruction word extension (See figure 7H: The mux 784 takes in multiple sectors and chooses which sector 722 to output).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Christie with Yates to incorporate multiplexers because multiplexers are recognized as one popular manner into which to select something from a set of values. It is very possible that Christie does intend to include multiplexers as it is a common device used by one having ordinary skill in the art at the time the invention was made but does not disclose the use of them. Yates does and one having ordinary skill in the art at the time the invention was made would appreciate such a device and would apply it to Christie.

As per claim 40, Christie does disclose the method as in claim 22.

Christie does not disclose using RISC instructions.

Yates does disclose where said instruction words comprise Reduced Instruction Set Computer (RISC) instructions (See column 22, 21-25: The processor disclosed is a RISC processor and thus will handle RISC instructions).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Christie with Yates a RISC instruction set was desired. Christie discloses a CISC instruction set as evidenced by the disclosure of an x86 instruction set (See Christie column 3, lines 31-33) and although it is very likely that the CISC instruction set is able to handle the RISC instruction set, Yates does explicitly disclose a RISC instruction set.

As per claim 41, Christie does disclose the method as in claim 40.

Christie does not disclose using RISC instructions.

Yates does disclose where said instructions words (See column 22, 21-25: The processor disclosed is a RISC processor and thus will handle RISC instructions) have a width of 32-bits (See column 38, lines 61-65: Yates, Jr. et al actually discloses a 64-bit processor, but it is well known in the art that backwards compatibility is built into processors and thus can handle 32-bit instructions as well), where extension to said at least one instruction word has a width of 8-bits (See column 24, lines 3-7: Variable length instructions are can be viewed as regular length instructions with extensions, include ones of 8-bits).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Christie with Yates a RISC instruction set was desired. Christie discloses a CISC instruction set as evidenced by the disclosure of an x86 instruction set (See Christie column 3, lines 31-33) and although it is very likely that the CISC instruction set is able to handle the RISC instruction set, Yates does explicitly disclose a RISC instruction set.

As per claim 42, Christie does disclose the method as in claim 41.

Christie does not disclose using RISC instructions.

Yates does disclose where said code page has a storage capacity of 4096 bytes (See column 61, lines 49-50), where said first section comprises 3072 bytes, and where said second section comprises 1024 bytes (See column 2, lines 36-49: Sections in pages are determined by flags and thus can be set to partition the 4096 bytes into 3072 and 1024 bytes).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Christie with Yates a RISC instruction set was desired. Christie discloses a CISC instruction set as evidenced by the disclosure of an x86 instruction set (See Christie column 3, lines 31-33) and although it is very likely that the CISC instruction set is able to handle the RISC instruction set, Yates does explicitly disclose a RISC instruction set.

Response to Arguments

8. Applicant's arguments, see Response to Office Action, filed 26 June 2006, with respect to the rejection(s) of claim(s) 1-44 under Yates, Jr et al (U.S. Patent # 6,397,379 B1) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Christie (U.S. Patent # 6,877,084 B1). Examiner would like to thank applicant for pointing out to where interpretation of claims was made incorrect, however, examiner feels the new grounds of rejection does indeed cover claims 1-44 given new interpretation of claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following are cited to show further art with respect to a method and apparatus to extend the number of instruction bits in processors with fixed length instructions, in a manner compatible with existing code:

U.S. Patent # 5,666,510 to Mitsuishi et al shows a data processing device having expandable address space.

U.S. Patent # 5,935,237 to Chiba et al shows a microprocessor capable of carrying out different data length instructions.

U.S. Patent # 6,314,504 B1 to Dent shows a multi-mode memory addressing using variable-length.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

vl
July 29, 2006

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
8/7/2006